CLAIMS

What is claimed is:

1. A method for pre-configuring an FPGA to a known state during a reset condition or prior to the FPGA undergoing system initialization, the method comprising:

loading a configuration value for an on-chip device of the FPGA into a flip-flop interconnected to said on-chip device; and

transferring said configuration value from said flip-flop to said on-chip device, said transfer of said configuration value effectuating pre-configuration of said on-chip device.

2. The method according to claim 1, further comprising pre-storing said configuration value in a memory cell of the FPGA.

3. The method according to claim 2, wherein said memory cell is a BRAM.

4. The method according to claim 2, further comprising transferring said configuration value from said memory cell to said flip-flop upon power-up of the FPGA.

5. The method according to claim 4, further comprising the supplying a clock signal to said flip-flop to effectuate said transfer of said configuration value from said memory cell to said flip-flop upon power-up of the FPGA.

6. The method according to claim 1, further comprising supplying a clock signal to said flip-flop to effectuate said

transfer of said configuration value from said flip-flop to said on-chip device.

7. The method according to claim 1, wherein said flip-flop is a D-type flip-flop.

8. The method according to claim 1, wherein said flip-flop is a configuration register for said on-chip device.

9. The method according to claim 1, wherein said on-chip device is an on-chip memory controller.

10. A method for pre-configuring an FPGA during a reset condition or prior to system initialization of the FPGA, the method comprising:

loading a value into at least one flip-flop of the FPGA, said at least one flip-flop functioning as a configuration register for an on-chip device of the FPGA; and

configuring said FPGA on-chip device to a particular state using said loaded value from said at least one flip-flop.

11. The method according to claim 10, wherein said loading step further comprises:

transferring said at least one value stored in at least one memory cell of the FPGA to said flip-flop; and

storing said transferred at least one value in said at least one flip-flop of the FPGA.

12. The method according to claim 11, wherein said loading step further comprises the step of loading said transferred at least one value into said at least one flip-flop whenever the FPGA is powered up.

13. The method according to claim 11, wherein the step of transferring further comprises storing said value for configuring said FPGA on-chip device in said at least one memory cell, said stored value representing a default state of said memory cell.

14. The method according to claim 10, wherein said at least one value is a bit.

15. A system for pre-configuring an FPGA to a known state during a reset condition or prior to the FPGA undergoing system initialization, the system comprising:

a flip-flop coupled to an on-chip device of the FPGA; and

a clock transitioning circuit coupled to said flip-flop for causing,

a configuration value for said FPGA on-chip device to be loaded into said flip-flop; and

said configuration value to be read by said on-chip device, said reading of said configuration value effectuating the pre-configuration of said on-chip device.

16. The system according to claim 15, further comprising an FPGA memory cell for pre-storing said configuration value.

17. The system according to claim 16, wherein said memory cell is a BRAM.

18. The system according to claim 15, wherein said flip-flop is a D-type flip-flop.

19. The system according to claim 15, wherein said flip-flop is a configuration register for said on-chip device.

20. The system according to claim 15, wherein said on-chip device is an on-chip memory controller.